DESCRIPTION

FERROELECTRIC MEMORY DEVICE

Technical Field

The present invention relates to ferroelectric memory devices and, more particularly, to structures of memory cell capacitors in the ferroelectric memory devices.

Background Art

A ferroelectric memory has a memory cell structure that is composed of a ferroelectric capacitor (hereinafter, also referred to as a memory cell capacitor) which holds polarity of applied voltage as data, and an access transistor (hereinafter, also referred to as a memory cell transistor) which executes data access to the memory cell capacitor. As a method of processing this memory cell structure, Japanese Published Patent Application No.2002-198494 discloses a method by which an upper electrode of the memory cell capacitor and a ferroelectric layer thereof are processed using the same mask, as an example.

Fig. 25(a) is a diagram for explaining a conventional ferroelectric memory device, and shows a layout of electrodes of ferroelectric capacitors which constituent memory cells. Fig. 25(b) is a cross-sectional view along the line XXVa-XXVa of fig. 25(a), and illustrates a cross-sectional structure of